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(71) Applicant: **Applied Materials, Inc.**
Santa Clara, California 95054 (US)

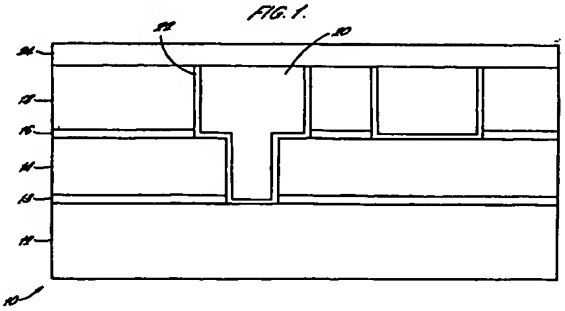
(72) Inventors:
- **Weidman, Timothy**
Sunnyvale, California 94086 (US)
- **Nault, Michael P.**
San Jose, Californis 95120 (US)
- **Chang, Josephine J.**
Carmichael, California 95608 (US)

(74) Representative:
Bayliss, Geoffrey Cyril et al
BOULT WADE TENNANT,
Verulam Gardens
70 Gray's Inn Road
London WC1X 8BT (GB)

(54) Capping layer for extreme low dielectric constant films

(57) A silicon-carbide-type or silicon oxycarbide (also often called carbon-doped-oxide [CDO] or organosilicate glass) capping material and method for depositing this capping material on ELK films which are used as a dielectric material in integrated circuits. The ELK film may include any ELK film including but not limited to inorganic, organic and hybrid dielectric materials and their respective porous versions. The silicon-carbide-type material may be an amorphous silicon carbide type material such as the commercially available BLOk™ material, or a carbon-doped oxide material such as the commercially available Black Diamond™ both of which are developed by Applied Materials of Santa Clara, Ca. The amorphous silicon carbide (a-SiC) material is deposited using a plasma process in a non-oxidizing environment and the CDO-type material is deposited using an oxygen-starved plasma process. The non-oxidative or oxygen-starved plasma processes do not significantly degrade the underlying film's chemical and electrical properties. The CDO material offers the advantageous property of having a lower dielectric constant value of less than 3.5 as opposed to the a-SiC material which has a dielectric constant of approximately 4.5. The CDO material besides, having a lower dielectric constant also has a superior adhesion characteristics to the underlying ELK material. However, experiments have indicated that despite its higher dielectric constant, the a-SiC-type material (e.g. BLOk™) may be used to generate capped ELK films with similar or even reduced dielectric constants relative to lower k capped films, and may provide composite (i.e. ELK+cap) structures exhibiting superior k stability.

FIG. 1.



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Description

[0001] The present invention relates to the formation of dielectric layers. More particularly, embodiments of the present invention relate to a method for capping a low dielectric constant film that is particularly useful as a premetal or intermetal dielectric layer in an integrated circuit.

[0002] Semiconductor device geometries have dramatically decreased in size since integrated circuits were first introduced several decades ago, and all indications are that this trend will continue. Today's wafer fabrication plants are routinely producing devices having 0.25μm and even. 0.18μm feature sizes, and the plants of the future will soon be producing devices having even smaller geometries.

[0003] The drive to faster and faster microprocessors, and more powerful microelectronic devices, is dependent on improvements in two chemistry-based areas, optical lithography and low dielectric constant materials. Several semiconductor manufacturers, materials suppliers and research organizations have focused on identifying low and extremely low dielectric constant films. As used herein, low dielectric constant materials are those films having a dielectric constant between 3.0 to 2.5 and extremely low dielectric constant ("ELK") films are those films having a dielectric constant below 2.5 extending to dielectric constants below 2.0.

[0004] Several candidate low dielectric constant materials are currently under development. Certain specific organic, inorganic and hybrid dielectrics arc amongst the current candidates. Additionally, dielectric films from these categories, when made porous, tend to have even lower dielectric constants, and are poised for integration in the next generation of interconnect structures. In terms of deposition techniques, both spin-on and chemical vapor deposition ("CVD") processes are under development, with key challenges remaining around issues of technological performance - i.e. integration.

[0005] Among the organic material candidates, organic polymers such as polyarylene and polyarylethers have been most intensively pursued. Two examples of such materials include porous versions of Dow Chemical's SiLK (a spin-on low k material (k between 2.6 - 2.8)] and FLARE from Allied Signal. Spin-on hydrogen silsesquioxane ("HSQ") which has a dielectric constant of 2.9 (k=2.9), is an example of an inorganic dielectric material. Hybrid materials combine organic and inorganic materials. In hybrid materials, cross-linked silicon-oxygen containing polymers designated as polysiloxanes form the basis for conventional spin-on-glass ("SOG") materials. One approach to achieving a lower dielectric constant in hybrid films has been to increase the amount of organic substitution in these materials . For example, where each silicon atom in a spin-on HSQ film is substituted with a methyl group, a methyl-silsesquioxane ("MSQ") results.

[0006] As stated above, incorporation of porosity in a dielectric film, regardless of its chemical composition, (i.e. organic, inorganic and hybrid) will reduce the film's dielectric value relative to the solid film. This is due to the fact that the dielectric constant of air is nominally 1. As a result dielectric constants are achievable that are lower than 2.5 including values less than 2.0.

[0007] One method of forming a particular type of ELK material which forms a porous oxide films is based on a sol-gel process, in which high porosity films are produced by hydrolysis and polycondensation of a silicon alkoxide such as tetraethylorthosilicate. The sol-gel process is a versatile solution process for making ceramic material. In general, the sol-gel process involves the transition of a system from a homogeneous liquid "sol" (mostly colloidal) into a solid "gel" phase. The starting materials used in the preparation of the "sol" are usually inorganic salts or compounds such as silicon alkoxides. The precursor solutions are typically deposited on a substrate by spin on methods. In a typical sol-gel process, the precursor is subjected to a series of hydrolysis and polymerization reactions to form a colloidal suspension, or a "sol." Further processing of the "sol" enables one to make ceramic materials in different forms. The further processing includes the thermal decomposition of a thermally labile component, which involves the formation of an ordered surfactant-templated mesostructured films by evaporation-induced self-assembly, followed by the thermal decomposition of the template.

[0008] In addition to requiring new materials for insulation layers, the trend of decreasing feature size in integrated circuits has created a need for a conductive material having greater conductivity than aluminum which has been the choice in the industry for some time. Many semiconductor manufacturers have turned to copper (Cu) as an interconnect material in place of aluminum, because copper has a lower resistivity and higher current carrying capacity. However, copper has its own difficulties for IC manufacturing processes. For instance, copper diffuses more readily into surrounding materials and hence requires better materials for a barrier layer than traditionally has been used for aluminum. This greater diffusion characteristic exacerbates the low k porosity described above and places even greater emphasis upon the quality of the barrier layers.

[0009] An example of an integrated circuit structure which implements copper as an interconnect material is a dual damascene structure. In a dual damascene structure, the dielectric layer is etched to define both the contacts/vias and the interconnect lines. Metal is inlaid into the defined pattern and any excess metal is removed from the top of the structure in a planarization process, such as chemical mechanical polishing (CMP). Figure 1 shows one example of a dual damascene structure. This structure is appropriate for a first intermetal layer. The integrated circuit 10 includes an underlying substrate 12, which may include a series of layers deposited thereon. The substrate 12 may have transistors therein. A barrier layer 13 may be deposited over the substrate, followed by a dielectric layer 14. The dielectric layer may be undoped silicon dioxide also known as undoped silicon glass (USG), fluorine-doped silicon glass (FSG), or a low k material such as a porous oxide layer or a silicon-carbon or carbon-doped silicon oxide film, or an ELK material. An etch stop layer 16 is deposited over layer 14, pattern etched, and followed by another dielectric layer 18. The structure is then again pattern etched to produce a damascene type

pattern. A barrier layer 22 may be needed, which typically has beet, made from Ta, TaN, Ti, TiN, silicon nitride and plasma enhanced chemical vapor deposited (PECVD) silicon dioxide. However, as explained above, with the smaller feature sizes and increased diffusion propensity of copper, the prior barrier layers arc inadequate for optimal performance. Once the conductive material 20 has filled the features, another layer 24, such as a passivation layer, may be deposited. The process described above for a dual damascene structure is exemplary and others may be more appropriate for other particular applications.

[0010] Such integration methods when using ELK material and especially porous dielectric materials place additional demands upon the liner or barrier layers. Liner or barrier layers including capping layers such as silicon nitride or silicon dioxide have been deposited adjacent to the low k dielectric layers to prevent the diffusion of byproducts such as moisture and copper. Silicon nitride has been one material of choice for passivation layers. However, silicon nitride has a relatively high dielectric constant (dielectric constant greater than 7.0) and may significantly increase the capacitive coupling between interconnect lines. High dielectric constants result in a capped insulator layer that does not significantly reduce the overall dielectric constant for the combined insulator-capping layer) which defeats the goals of reducing the dielectric constant of the insulating material. Similarly, problems remain in depositing a silicon dioxide capping layer on a porous film. The capping layer is typically deposited in an oxidative PECVD process. Such an oxidative process damages the surface functionality of the underlying porous film and results in degrading the underlying film's chemical properties, which can degrade the low dielectric constant properties of the film. In addition, although silicon-carbide-type material are known to be appropriate for use as barrier or etch stop layers, their use in IC structures using ELK materials and especially porous ELK materials does riot appear to be suitable. This is because the lower k silicon carbide-type materials (such as the commercially available Black Diamond™ [k less than 3.0] developed by Applied Materials of Santa Clara, Ca.) are also typically deposited in an oxidative PECVD process, which as described above could damage the underlying porous film, and the higher k silicon-carbide-type films (such as the commercially available BLOk material ™ [k less than 4.5] also developed by Applied Materials of Santa Clara, Ca.) may not be suitable because their k value is too high, which could result in an overall capped ELK film stack having too high of a k value.

[0011] Therefore, there is a need for a capping layer that will have the lowest dielectric constant possible and one whose deposition process does not damage the underlying ELK film or degrade the underlying film's chemical properties.

[0012] Embodiments of the present invention provide a silicon-carbide-type or silicon oxycarbide (also often called carbon-doped-oxide [CDO] or organosilicate glass) capping material and method for depositing this capping material on ELK films which are used as a dielectric material in integrated circuits. The ELK film may include any ELK film including but not limited to inorganic, organic and hybrid dielectric materials and their respective porous versions. The capping material may be amorphous silicon carbide type material such as the commercially available BLOk™ material, or a carbon-doped oxide material such as the commercially available Black Diamond™ both of which are developed by Applied Materials of Santa Clara, Ca. The amorphous silicon carbide (a-SiC) material is deposited using a plasma process in a non-oxidizing environment and the CDO-type material is deposited using an oxygen-starved plasma process. The CDO material offers the advantageous property of having a lower dielectric constant value of less than 3.5 as opposed to the a-SiC material which has a dielectric constant of approximately 4.5. The CDO material besides, having a lower dielectric constant also has a superior adhesion characteristics to the underlying ELK material. Additionally, the non-oxidative or oxygen-starved plasma processes do not significantly degrade the underlying film's chemical and electrical properties. However, experiments have indicated that despite its higher dielectric constant, the a-SiC-type material (e.g. BLOk™) may be used to generate capped ELK films with similar or even reduced dielectric constants relative to lower k capped films, and may provide composite (i.e. ELK+cap) structures exhibiting superior k stability.

[0013] These and other embodiments of the present invention, as well its advantages and features, are described in more detail in conjunction with the description below and attached figures.

Fig. 1 is a simplified cross-sectional view of a portion of an integrated circuit having a dual damascene structure.

Fig. 2 is a flowchart of a process in which a capped ELK layer is formed.

Fig. 3 is a flowchart of a typical process in which a templated sol-gel process is used to deposit a porous silicon oxide layer.

[0014] Embodiments of this invention provide a method to deposit a silicon carbide type low dielectric constant film as a capping layer or a carbon doped silicon oxide film as a capping layer or a combination thereof over an extremely low dielectric constant ("ELK") film that may contain oxidizable $Si-CH_3$ and or Si-H groups. The capping layer is deposited using a PECVD process in either a non-oxidizing or an oxygen starved plasma. Both the non-oxidizing and the oxygen starved plasma processes prevent or minimize oxidation of the underlying ELK film.

[0015] The lack of an oxidizing plasma in the PECVD deposition process allows the capping layer to be deposited without degrading the ELK film, Using process conditions described below capping layers having a dielectric constant below 5 and preferably below 3 is deposited on an ELK film. Using these process conditions, the deposition regime of the capping layer does not oxidize the $Si-CH_3$ or Si-H bonds in the ELK film, and thus allows for a dielectric

constant for the combined ELK film and capping layer stack to be less than 3.0. As used herein a capping layer may be a metal diffusion barrier, an etch stop layer, a CMP stop layer, a photoresist barrier or a final passivation layer.

[0016] Fig. 2 is a high-level flowchart of a process for forming a capped ELK layer on a substrate according to an embodiment of the present invention. As shown in Fig. 2, first a substrate is placed in a processing chamber (step 200). Next, an ELK material is formed on the substrate (step 210) and finally the ELK layer is capped by a silicon carbide layer, or alternately by a CDO-type layer, or by a combination of a silicon carbide and a CDO layer (step 220). The chamber used to deposit and the one used to cap the film are not the same chamber since the ELK film is a spin-on film and the cap layer a CVD film. ELK films are porous and are faced with more challenging downstream wafer processing integration issues. As described above, integration issues encompass many wafer processing steps including those described above for a dual damasccne process and which may include photoresist depositior, metalization, etch, and CMP. This means that subsequent processes must not damage the underlying ELK film and subsequently deposited films must be isolated from the underlying ELK. Therefore, a capping layer and its method of deposition on an ELK film must not degrade the underlying film's desired properties. Furthermore, the capping layer should preferably posses a low dielectric constant value to ensure that the gains made in depositing an ELK film are not adversely offset by capping it with a high dielectric constant film and effectively increasing the overall dielectric constant for the capped film stack.

[0017] Before describing the capping layer and a method of depositing the capping material according to embodiments of the present invention, an exemplary ELK material and process for its deposition also in accordance with embodiments of the present invention is described below.

Exemplary ELK Material and Methods For Its Deposition

[0018] An exemplary process for forming an ELK layer is based on a sal-gel process. In such a particular sol-gel process for forming a porous low dielectric constant film, surfactants act as the template for the film's porosity. The porous film is generally formed by the deposition on a substrate of a sal-gel precursor followed by selective evaporation of solvent components of the sol-gel precursor to form supramolecular assemblies. The assemblies are then formed into ordered porous films by the pyrolysis of the supramolecular surfactant templates at approximately 400°C.

[0019] Figure 3 is a flowchart illustrating a basic sol-gel process that has been previously proposed to deposit ELK films. As shown in Fig. 3, the first step is the synthesis of the stock precursor solution (step 300). The stock precursor solution is prepared, for example, by combining a soluble silicon oxide source, e.g., TEOS (tetraethoxysilane), water, a solvent, e.g. alcohol, arid an acid catalyst, e.g. hydrochloric acid, in particular mole ratios at certain prescribed environmental conditions and mixed for certain time periods.

[0020] Once the stock solution is obtained, the coating solution is mixed (step 310). The general procedure to prepare the coating solution is to add a surfactant to the stock solution. The surfactants are used as templates for the porous silica, In later processes the surfactants are baked out, leaving behind a porous silicon oxide film. Typical surfactants exhibit an amphiphilic nature, meaning that they can be both hydrophilic and hydrophobic at the same time. Amphiphilic surfactants possess a hydrophilic bead group or groups which have a strong affinity for water and a long hydrophobic tail which repels water. The long hydrophobic tail acts as the template member which later provides the pores for the porous film. Amphiphiles can aggregate into supramolecular arrays which is the desired structure that needs to be formed as the template for the porous film. Templating oxides around these arrays leads to materials that exhibit controllable pore sizes and shapes. The surfactants can be anionic, cationic, or nonionic, though for the formation of dielectric layers for IC applications, non-ionic surfactants are generally preferred. The acid catalyst is added to accelerate the condensation reaction of the silica around the supramolecular aggregates.

[0021] After the coating solution is mixed it is deposited on the substrate (step 320) using a spinning process where centrifugal draining ensures that the substrate is uniformly coated with the coating solution. The coated substrate is then pro-baked to complete the hydrolysis of the TEOS precursor, continue the gelation process, and drive off any remaining solvent from the film (step 330).

[0022] The pre-baked substrate is then further baked to form a hard-baked film (step 340). The temperature range chosen for the bake step will ensure that excess water is evaporated out of the spin cast film. At this stage the film is comprised of a hard-baked matrix of silica and surfactant with the surfactant possessing an interconnected structure characteristic of the type and amount of surfactant employed. The interconnected structure aids the implementation of the subsequent surfactant extraction phase. The interconnected structure provides continuous pathways for the subsequently ablated surfactant molecules to escape from the porous oxide matrix.

[0023] Typical silica-based films often have hydrophilic pore walls and aggressively absorb moisture from the surrounding environment. If water, which has a dielectric constant (k) of about 78, is absorbed into the porous film, then the low k dielectric properties of the film can be detrimentally affected. Often these hydrophilic flints are annealed at elevated temperatures to remove moisture and to ablate and extract the surfactant out of the silica-surfactant matrix. Such an anneal step leaves behind a porous film exhibiting interconnected pores (step 350). But this is only a temporary solution in a deposition process since the films may still be sensitive to moisture absorption following this procedure.

[0024] Some sol-gel processes include further post-deposition treatment steps that are aimed at modifying the surface characteristic of the pores to impart various desired properties, such as hydrophobicity, and increased resistance to certain chemicals. A typical treatment that renders the film more stable is treatment with HMDS

(hexamethyldisilizane, $[(CH_3)_3\text{-}Si\text{-}NH\text{-}Si\text{-}(CH_3)_3]$), in a dehydroxylating process which will remove the hydroxyl groups, replace them with trimethysilyl groups, and render the film hydrophobic (step 360). Alternatively, or in conjunction with such a silylation step, the porous material may be rendered more hydrophobic by the addition of an alkyl substituted silicon precursor, such as $CH_3Si(OCH_2CH_3)$ methyl triethoxysilane or MTES to the precursor formulation.

[0025] A variety of alternatives to the above described sol-gel process for depositing low k material have been proposed. Many of these alternatives follow the same basic general approach discussed above but vary the choice of ingredients used in the coating solution; the processing times and/or temperatures; combine certain steps; and/or divide other steps into various substeps.

[0026] For example, an alternate process for depositing and forming a hardened and stable ELK film according to an embodiment of the present invention is provided below. Using this alternate process, an ELK film was deposited based on a sal-gel-based process as described above by steps 300-350. During steps 300-350 a precursor solution containing at least a silica precursor composed primarily of a silicon/oxygen compound, water, a solvent, a surfactant and a catalyst was formed. The precursor solution was spun on the wafer and the wafer thermally treated by being baked in a chamber at various temperatures between 90°C to 450 °C for between 30 to 3600 seconds in inert or oxidizing environments having pressures in the range from 0.1 Torr to atmospheric. The silicon/oxygen compound was selected from the group consisting tetraethylorthosilicate, tetramethoxy silane, phenlytriethyloxy, methyltriethoxy silane and combinations thereof, The solvent was selected from the group consisting of ethanol, isopropanol, propylene glycol monopropyl ether, n-propanol, n-butanol, t-butauol, ethylene glycol and combinations thereof. The surfactant was a non-ionic surfactant selected for example from the group consisting of polyoxythylene oxides- propylene oxides-polyethylene oxides triblock copolymers, octaethylene glycol monodecyl ether, octaethylene glycol monohexadecyl ether. Triton™ 100, Triton™ 114 and related compounds and combinations thereof. More particularly, the precursor solution used in embodiments of this invention has the following composition: tetraethoxysilane (TEOS) - 22.5 gms; methyltriethoxysilane (MTES) - 22.5 gms; propylene glycol monopropyl ether (PGPE) - 100 gms; 0.1N Nitric acid - 24 gms; tetramethylamonium hydroxide (TMAH)(2.4% in water) - 1.0 gms; and Triton X-114 - 9.67 gms (Triton 114 is trademark of a mixture of ethoxylated p-tert-octylphenols manufactured by the Union Carbide Corporation).

[0027] As can be recognized, numerous alternate embodiments of the ELK film may be deposited depending upon the choice of the spin-on solution ingredients and processing times and parameters. The ELK film deposited according to the embodiments of this process exhibits the following properties:

- the film is composed essentially of Si-O and $Si\text{-}CH_3$ bonds
- a dielectric constant in the range between 1.6 and 2.3
- a porosity between 20% to 60%
- a modulus of elasticity of between 1.4 to 10 GPa, and generally between 3 to 6 GPa
- a hardness value between 0.4 and 2.0 GPa, and generally between 0.5 and 1.2 GPa
- a refractive index at 633 nm of between 1.1 to 1.5

[0028] One apparatus that can be used for the atmospheric deposition of ELK films according to the embodiments of the invention described above is described in copending patent application Serial number 09/502,126, assigned to the assignee herein, and titled: A PROCESS AND AN INTEGRATED TOOL FOR LOW K DIELECTRIC DEPOSITION INCLUDING A PECVD CAPPING MODULE; which is hereby incorporated herein in its entirety.

[0029] Having described examples of particular ELK films, materials and methods of capping such films is described below. While it has become apparent that forming ELK films having k<2.5 is feasible, such films which are porous are faced with more challenging downstream wafer processing integration issues, which require unique methods and materials to isolate these ELK films from other layers. As described above, a capping layer and its method of deposition on an ELK film must not degrade the underlying film's desired properties. Furthermore, the capping layer should preferably posses a low dielectric constant value to ensure that the gains made in depositing an ELK film are not adversely offset by capping it with a high dielectric constant film and effectively increasing the overall dielectric constant for the capped film stack.

SiC and CDO Materials As Capping Layers For ELK Films

[0030] Embodiments of the present invention provide a silicon-carbide-type or alternately a silicon oxycarbide (also often called carbon-doped-oxide [CDO] or organosilicate glass) capping material, formed according to certain process regimes useful as a capping layer for an integrated circuit, and particularly for an integrated circuit using copper as a conductive material and ELK films as dielectrics. The capping material may be an amorphous silicon carbide type material such as the commercially available BLOk™ material, or a carbon-doped oxide material such as the commercially available Black Diamond™ both of which are developed by Applied Materials of Santa Clara, Ca. The

amorphous silicon carbide (a-SiC) material is deposited using a plasma process in a non-oxidizing environment and the CDO-type material is deposited using an oxygen-starved plasma process. The CDO material offers the advantageous property of having a lower dielectric constant value of less than 3 as opposed to the a-SiC material which has a dielectric constant of approximately 4.5. The CDO material besides, having a lower dielectric constant also has a superior adhesion characteristics to the underlying ELK material. Additionally, the non-oxidative or oxygen-starved plasma processes do not significantly degrade the underlying film's chemical and electrical properties because at these oxygen levels the plasma processes do not result in the complete oxidation of the organosilane or the organic component of the underlying ELK film. However, experiments have indicated that despite its higher dielectric constant, the a-SiC-type material (e.g. BLOk™) may be used to generate capped ELK films with similar or even reduced dielectric constants relative to lower k capped films, and may provide composite (i.e. ELK+cap) structures exhibiting superior k stability. The process conditions and experimental results are described below.

[0031] As described above, and used herein, a capping layer can be a barrier layer, an etch stop, a CMP slop, or other barrier layer isolating an underlying ELK film from other material subsequently deposited or etched. Embodiments of the present invention also provide processing regimes that include using a silane-based compound for a silicon source in some embodiments and an organosilane as a silicon and carbon source and potentially in the absence of a substantial amount of oxygen. The process regimes also include the presence of inert gases, such as helium or nitrogen, and at certain temperatures, pressures, power outputs in a PECVD chamber to produce the capping material according to embodiments of the present invention. This particular capping material is especially useful as a capping layer for an ELK film, and may be especially useful in complex structures, such as a damascene structure.

[0032] Table 1 below shows some general requirements for a capping layer using copper as a conductive material, although other conductors may be applicable.

Table 1

DESIRABLE CHARACTERISTICS OF DIELECTRIC CAPPING LAYER	
Good Adhesion	• Adhesion to Underlying (ELK Film) and Overlying Layers
Not Degrade Underlying Film	• Non-oxidizing Deposition Process
Good Barrier Property to Copper	• No Copper diffusion at 400°-450°C
Lower Dielectric Constant	• Overall Low Dielectric Constant (K) in IMD Damascene Stack
Adjustable (High or Low) Etch Selectivity with respect to ELK Film	• Tuned Composition to match or contrast ELK Film to Effect Selectivity
Good Electrical Properties	• High breakdown Voltage • Low Leakage

Desirable Characteristics of Dielectric Capping Material

[0033] Referring to Table 1, adequate adhesion between layers is required to avoid or reduce delamination between them. A measure of adhesion strength is the stud pull test. Using this criteria, an adhesion strength greater than 35 MPa is desired, and tests showed that an adhesion strength of at least 35 MPa was obtained for the capping layer when deposited in accordance with the process described below. The capping material must be such that its deposition process does not degrade the underlying ELK film. This critaria is satisfied by depositing the capping material from a non-oxidizing or oxygen-poor plasma. In case of the oxygen-poor plasma, all or most of the oxygen in the process gas should be consumed in the reaction with the organolsilane such that no oxygen is left free to react with the chemical structure of the underlying ELK film. The capping material should also have substantially no diffusion at substrate annealing temperature of, for example, 400°- 450° C. The term "no substantial" diffusion is intended to be a functional term, such that any actual diffusion into the layer is less than would affect the ability of the capping layer to function as such. For instance, the silicon carbide of an embodiment of the present invention limits the diffusion to about 250Å. The copper diffusion may impair the desired current and voltage paths and contribute to cross-talk. Because of the decreasing feature size, as described above, the lower dielectric constant, preferably less than 5, the lower the probability for cross talk and RC delay which degrades the overall performance of the device. Related to the low dielectric value of the film is the overall stack dielectric value, which corresponds to the overall dielectric value of the combined capped ELK film (i.e. ELK film and capping layer), where a desirable value should be 3.0 or less.

[0034] Because the barrier layer may be used in a damascene structure, it would be beneficial to also have suitable etch stop characteristics, such as an etch selectivity ratio of 1:3 or preferably lower with respect to ELK materials. On the other hand, it may be advantageous to tune the composition of the capping layer to match that of the ELK film to have a low etch selectivity and hence allow for single pass etch of the capping layer and the ELK film. A low etch selectivity may be used in which a via pattern is transferred through the capping layer and into the ELK film at the same time the photoresist is removed. Additionally the capping material should have a high breakdown voltage of 2 MV/cm or more. It should also have a low leakage through the layer, i.e., a low stray direct current that capacitively flows through the material. Another desired characteristics from a commercial standpoint

is that the material should be compatible with other processes, so the processes may be conducted in-situ. i.e. in a. given chamber, such as in a an integrated cluster tool arrangement,, without exposing the material to a contaminating environment, to produce better throughput and process control. This aspect may be particularly important with ELK films, because of their porosity and susceptibility to moisture absorption.

[0035] Table 2 below shows the process parameters used in a chamber that allows the film to be used as a capping layer in accordance with the embodiments of the present invention. In the embodiments tested, the silicon and carbon were derived from a common compound, such as an organosilane-based compound. However, the carbon could be supplemented with other compounds, such as methane. Without limitation, suitable silane-based compounds could include: methylsilane (CH_3SiH_3), dimethylsilane ($(CH_3)_2SiH_3$), trimethylsilane ($(CH_3)_3SiH_3$), diethylsilane ($(C_2H_5)_2SiH_2$), propylsilane ($C_3H_8SiH_3$), vinyl methylsilane ($(CH_2=CH)CH_3SiH_2$), 1, 1, 2,2-tetramethyl disilane ($HSi(CH_3)_2$-$Si(CH_3)_2H$), hexamethyl disilane ($(CH_3)_3Si$-$Si(CH_3)_3$), 1, 1, 2, 2, 3, 3-hexamethyl trisilane ($H(CH_3)_2Si$-$Si(CH_3)_2$-$SiH(CH_3)_2$), 1, 1, 2, 3, 3-pentamethyl trisilane ($H(CH_3)_2Si$-$SiH(CH_3)$-$SiH(CH_3)_2$), and other silane related compounds. In addition to organosilanes exemplified by the above list, orgaxiosiloxanes such as tetramethyl cyclotetrasiloxane may be used, with or without the addition of another oxygen source, for the deposition of CDO type caps. For the purpose of this invention, the term "organosilane" as used herein includes any silane-based compound having at least one carbon atom attached, including the preceding list, unless other wise indicated. In Table 2, the compounds used was trimethylsilane ("3MS"). A process gas, such helium, nitrogen, or oxygen was present and may assist in stabilizing the process, although other gases could be used.

Table 2

Parameter	Range	CDO	a-SiC	a-SiC + CDO	
				Dep 1: a-SiC;	Dep 2: CDO
Silicon and Carbon (3MS)	50-2400 sccm (6 X oxygen flow)	600 sccm	160 sccm	300 sccm	600 sccm
Oxygen	0-400 sccm	100 sccm	0	0	100 sccm
Helium	0-5000 sccm	0	400 sccm	0	0
Nitrogen	0-5000 sccm	0	0	0	0
RF Power	100-900 W	590 W	560 W	300 W	590 W
Pressure	1-15 Torr	3.8 Torr	8.7 Torr	3.8 Torr	3.8 Torr
Temperature	350° - 450° C	400° C	400° C	400° C	400° C
Spacing	200-600 mil	280 mil	280 mil	230 mil	280 mil

Process Parameters for Capping Layer Deposition

[0036] The inventors have discovered that the process regime described above establishes the suitability of the capping material in meeting the desired criteria of a capping layer for ELK films. As used herein, the capping material includes both the a-SiC and the CDO materials. Using these process regimes, the capping layer can have a low dielectric constant of about 5 or less and can be extended to 3.5 or less by addition of some oxygen. Moreover, the effective dielectric constant of the stack composed of the ELK layer and the cap layer can be less than 2.5 for relatively thin cap layers. This effective dielectric constant meets the needs of a suitable capping layer especially for an ELK and copper-based integrated circuit. The capping material is also suitable as a low k, etch stop material. A low k etch stop material is defined herein as an etch stop material having a dielectric constant equal to or lower than that of silicon nitride (dielectric constant greater than or equal to 7.0) and having a relative oxide to etch selectivity of 2 to 1 or greater. This ratio allows greater control over the etching process and is particularly useful when etching complex structure, such as a damascene structure. Also by tuning the composition of the capping layer to match that of the ELK film, thus having a low etch selectivity allows for single pass etch of the capping layer and the ELK film. A low etch selectivity may be used such that a via pattern is transferred through the capping layer and into the ELK film at the same time the photoresist is removed.

[0037] To form the capping layer in the preferred process regime, a silicon source such as trimethylsilane may be supplied to a plasma reactor, specifically a reaction zone in a chamber that is typically between the substrate surface and the gas dispersion element, such as a "showerhead," commonly known to those with ordinary skill in the art. Typical commercial PECVD chambers that may be used to practice embodiments of this invention to cap an ELK film, are the DXz and Producer chambers produced by Applied Materials, Inc. of Santa Clara, California Alternately, the entire stack (i.e. formation of ELK film and PECVD cap) may be formed in a integrated atmospheric deposition and vacuum cap system as described above. The sequence of operation of a commercial PECVD chamber is well known

and needs no explanation for the embodiments of the present invention process regimes.

CDO Cap Deposition

[0038] Using such a PECVD chamber, a precursor source such as a trimethylsiline may be provided at a flow rate of about 600 standard cubic centimeters per minute (sccm). The reaction may occur without a substantial source of oxygen introduced into the reaction zone, more particularly a flow of 100 sccm of oxygen gas is used. In conjunction with the silicon and carbon sources, a process gas, such as helium or nitrogen, may flow into the chamber at a rate of about 0-5000 sccm each respectively. The chamber pressure is maintained between 1 to 15 Torr, and more particularly 3.8 Torr. An RF power source may apply between 100 to 900 watts, and preferably about 590 watts to the anode and cathode to form the plasma in the chamber with the silane-base gas. The substrate surface temperature may be maintained between about 300° to 450°C, and more particularly about 400 °C during the deposition of the capping layer. The gas may be dispersed at a showerhead to substrate spacing distance between 200 to 600 mils, and more particularly at 280 mil. Using this recipe a deposition rate of approximately 3700 Å/min is achieved. The measured thickness for the combined capped ELK film was approximately 5270 Å, and the dielectric constant for the capped ELK film was 2.38. The ELK film's dielectric constant was measured to be 2.16. Alternately, an ELK film was capped with a layer of a-SiC material as described below.

a-SiC Cap Deposition

[0039] Using such a PECVD chamber, a silicon carbide source such as a trimethylsilane may be delivered at a flow rate of about 160 standard cubic centimeters per minute (sccm). The reaction occurs without any source of oxygen introduced into the reaction zone. In conjunction with the trimethylsilane (silicon and carbon sources), a process gas, such as helium or nitrogen, may flow into the chamber at a rate of about 0-5000 sccm each respectively, more particularly, a flow of 400 sccm of helium is used. The chamber pressure is mantained between 1 to 15 Torr, and more particularly 3.8 Torr. An RF power source may apply between 100 to 900 watts, and preferably about 560 watts to the anode and cathode to form the plasma in the chamber with the silane-base gas. The substrate surface temperature may be maintained between about 350° to 450°C, and more particularly about 400 °C during the deposition of the capping layer. The gas may be dispersed at a showerhead to substrate spacing distance between 200 to 600 mils, and more particularly at 280 mil. Using this recipe a deposition rate of approximately 3700 Å/min is achieved. The measured thickness for the combined capped ELK film was approximately 5222 Å, and the dielectric constant for the capped ELK film was 2.22. The ELK film's dielectric constant was measured to be 2.16. Alternately, an ELK film may be capped with a combined capping layer by first depositing an a-SiC cap followed by CDO cap as described below.

Combined a-SiC and CDO Cap Deposition

[0040] For the first deposition, namely the a-SiC deposition, a silicon carbide source such as a trimethylsilane may be provided at a flow rate of about 300 standard cubic centimeters per minute (sccm). The reaction occurs without any oxygen introduced into the reaction zone, The chamber pressure is maintained between 1 to 15 Torr, and more particularly 3.8 Torr. An RF power source may apply between 100 to 900 watts, and preferably about 300 watts to form the plasma in the chamber with the trimethylsilane. The substrate surface temperature may be maintained between about 350° to 450°C, and more particularly about 400 °C during the deposition of the a-SiC capping layer. The gas may be dispersed at a showerhead to substrate spacing distance between 200 to 600 mils, and more particularly at 280 mil. Next, a CDO cap is deposited on the a-SiC cap. Using the same PECVD chamber, an organosilane such as trimethylsilane at a flow rate of about 600 standard cubic centimeters per minute (sccm) may be used. The carbon may be derived from the trimethylsilane or methylsilane. The reaction may occur without a substantial source of oxygen introduced into the reaction zone, more particularly a flow of 100 sccm of oxygen gas is used. The chamber pressure is maintained between 1 to 15 Torr, and more particularly 3.8 Torr. An RF power source may apply between 100 to 900 watts, and preferably about 600 watts to the anode and cathode to form the plasma in the chamber. The substrate surface temperature may be maintained between about 350° to 450°C, and more particularly about 400 °C during the deposition of the capping layer. The gas may be dispersed at a showerhead to substrate spacing distance between 200 to 600 mils, and more particularly at 280 mil. Using this recipe a deposition rate of approximately 3700 Å/min is achieved. The measured thickness for the combined capped ELK film was approximately 5107 Å, and the dielectric constant for the capped ELK film was 2.15. The ELK film's dielectric constant was measured to be 2.16.

[0041] As described above, The capping layer may be a film such as the commercially available BLOk™ material, or a CDO type film compound such as the commercially available Black Diamond™ both of which are developed by Applied Materials of Santa Clara, Ca. The a-SiC compound is deposited using a plasma process in a non-oxidizing environment and the CDO compound is deposited using an oxygen-starved plasma process.

[0042] The advantages of such a capping layer for ELK films as compared to traditional capping layers such as silicon oxide and silicon nitride are numerous. The non-oxidative or alternately the oxygen-starved process regime of embodiments of the present invention do not allow any substantial reaction between the plasma and the Si-C, C-H, and Si-H (if any) bonds present in the underlying ELK film and thus no substantial degradation in the ELK film's desirable dielectric and moisture-repelling properties is observed. Depositing silicon oxide as a capping layer in an oxidizing plasma environment would burn out the carbon in the ELK film, and degrade the ELK film's desirable properties. A set of tests carried out by the inventors, where a 1000 Å SiC capping layer was deposited on a 5000 Å

ELK film, showed that overall stack dielectric values of 3.0 or less where achieved, which indicate that the deposition recipe, described below, does not adversely impact the ELK film's properties. The ELK layer alone had a k of 2.0.

[0043] Additional tests carried out by the inventors using processes described above, involved the capping of the ELK film with three different capping layers. The first capping layer was the CDO cap; the second was the a-SiC cap, and the third was a two layer cap consisting of first capping the ELK film with an a-SiC cap and then with a CDO layer. The process conditions used for these tests are described above. The results of these experiments were quite unexpected in that the overall dielectric constant of the capped ELK film which was capped with a higher dielectric constant cap was actually lower than the overall dielectric constant of the capped ELK film which was capped with a lower dielectric constant cap.

[0044] The CDO material offers the advantageous property of having a lower dielectric constant value of less than 3 as opposed to the a-SiC material which has a dielectric constant of approximately 4.5. Additionally, the oxygen-starved plasma processes do not significantly degrade the underlying film's chemical and electrical properties. However, as stated above, experiments have indicated that despite its higher dielectric constant, the a-SiC-type material (e.g. BLOk™) may be used to generate capped ELK films with similar or even reduced dielectric constants relative to lower k capped films, and may provide composite (i.e. ELK+cap) structures exhibiting superior k stability. These experiments support the unexpected result that flints capped with the higher k SIC type film give bettor overall k values and k stability for the stack than films capped with the lower k SiC material. The inventors believe that this is due fact that the lower k cap (CDO) deposition may induce some oxidation of the underlying ELK film during the deposition process. Also because of the oxidation of the ELK film and the lower effectiveness of CDO layers as moisture barriers, the k stability for the ELK-CDO stack is worse than the ELK-a-SiC stack, as shown in Table 3 below.

Table 3

Wafer ID	Description	k	k after H2O	% k increase
356	Elk	2.16	2.28	5.9
247	Elk, CDO	2.38	2.47	3.6
244	Elk, a-Si-C	2.22	2.25	1.6
354	Elk, a-Sic - CDO	2.15	2.21	2.8

Summary Results of SiC Capped ELK Films

[0045] The results summarized in Table 3 above, are unexpected in that one would anticipate that a flint stack consisting of an ELK film and a capping layer would exhibit a lower overall k when capped with a lower k capping layer. It is know that CDO films have a lower k (approximately 3) as compared to a-SiC films (approximately 4.5). However as the results of experiments show, the ELK film capped with the a-SiC exhibits a lower over all k. AS shown above, the ELK film stack capped with an a-SiC material has an overall k of 2.22 as compared to the film stack capped with a C

[0046] Other capping materials such as the traditional silicon nitride cap has a relatively high dielectric constant. Although the high dielectric value could be addressed by depositing a relatively thin layer, its deposition can involve the use of an ammonia-based (NH_3) process gas. Such a process gas also reacts with and is detrimental to the underlying ELK film. Lastly and importantly, the adhesion between silicon-carbide type films as taught by the embodiments of the present invention are superior to other PECVD-based films. For example, the SiC material of the present invention has a high adhesion strength with test data showing an adhesion strength of greater than 5 Kpsi.

[0047] Having fully described several embodiments of the method of the present invention for depositing and capping a particular type of ELK film as described above, many other equivalent or alternative methods of depositing and capping ELK layers according to the present invention will be apparent to those skilled in the art. Additionally, the capping layer and the method of depositing the capping layer as described herein are equally applicable and equally advantageous as capping layers for other low dielectric constant or other ELK films. Low dielectric constant or ELK films other than the hybrid carbon doped porous oxide ("CDPO") described above can be other hybrid, organic and inorganic films including the porous variants thereof. Examples of organic films are Dow Chemical's SiLK (a spin-on low k material (k between 2.6 - 2.8) and FLARE from Allied Signal, and porous versions of these films. Examples of other hybrid films are HSQ and MSQ films and their respective porous variants. These equivalents and alternatives are intended to be included within the scope of the present invention which is set forth in the following claims.

Claims

1. A process for capping an extremely low dielectric constant ("ELK") film using a silicon carbide type film comprising:

forming an ELK film on a substrate, and

depositing a silicon carbide capping layer on said ELK film.

2. A process as claimed in claim 1 further comprising producing a silicon carbide layer having a dielectric constant of less than approximately 5.

3. A process as claimed in claim 1, wherein said silicon carbide capping layer is a carbon doped oxide capping layer having a dielectric constant of less than approximately 3.5.

4. A process as claimed in any of claims 1 to 3, further comprising producing a silicon carbide capping layer which is copper diffusion resistant.

5. A process as claimed in any of claims 1 to 4, wherein a deposition process for depositing said silicon carbide capping layer does not adversely react with said ELK film to substantially degrade said ELK film's dielectric property.

6. A process as claimed in any of claims 1 to 5, wherein said silicon carbide capping layer has an adhesive strength to said ELK film of greater than 35 Mpa.

7. A process as claimed in any of claims 1 to 6, further comprising a silicon carbide capping layer having no substantial penetration of moisture.

8. A process as claimed in any of claims 1 to 7, further comprising producing a combined dielectric constant for a stack consisting of said ELK film and said silicon carbide capping layer to be less than 3.0.

9. A process as claimed in any of claims 1 to 8, further comprising producing a combined dielectric constant for a stack consisting of said ELK film and said silicon carbide capping layer to be less than 2.5.

10. A process as claimed in any of claims 1 to 9, wherein said ELK film has a dielectric constant of approximately 3.0 or less.

11. A process as claimed in any of claims 1 to 10, wherein said ELK film has a dielectric constant of approximately 2.5 or less.

12. A process as claimed in any of claims 1 to 11, wherein said silicon carbide capping layer is deposited by:

introducing a silicon containing precursor, a carbon containing precursor, and a process gas into a chamber, wherein said process gas comprises oxygen, helium and nitrogen;

initiating a plasma in said chamber;

reacting said silicon containing precursor and said carbon containing precursor in the presence of said plasma to form silicon carbide; and

depositing a silicon carbide capping layer on said ELK film.

13. A process as claimed in claim 12, wherein said silicon containing precursor comprises a silane.

14. A process as claimed in claim 12, wherein said silicon containing precursor and carbon containing precursor are derived from a common organosilane precursor.

15. A process as claimed in claim 14 further comprising providing said organosilane precursor at a rate approximately six times that of the flow of oxygen gas.

16. A process as claimed in any of claims 13 to 15, wherein the silane is methylsilane.

17. A process as claimed in claim 16, further comprising providing said methylsilane at a rate approximately between 5-2400 sccm.

18. A process as claimed in claim 16 or claim 17, further comprising providing said methylsilane at a rate approximately between 100-650 sccm.

19. A process as claimed in any of claims 12 to 18, further comprising depositing said silicon carbide capping

layer at a temperature of between approximately 100° to 450°C.

20. A process as claimed in any of claims 12 to 19, further comprising depositing said silicon carbide capping layer at a temperature of between approximately 375° to 425°C.

21. A process as claimed in any of claims 12 to 20, further comprising depositing said silicon carbide capping layer at a pressure between approximately 1 to 15 Torr.

22. A process as claimed in any of claims 12 to 21, further comprising depositing said silicon carbide capping layer at a pressure between approximately 2 and 5 Torr.

23. A process as claimed in any of claims 12 to 22, wherein reacting said silicon and carbon comprises reacting said silicon and carbon using an RF power supply providing a power between approximately 100 to 900 watts.

24. A process as claimed in any of claims 12 to 23, wherein reacting said silicon and carbon comprises reacting said silicon and carbon using an RF power supply providing a power between approximately 300 to 600 watts.

25. A process as claimed in any of claims 12 to 24, wherein reacting said silicon and carbon comprises reacting said silicon and carbon using an RF power supply providing a power between approximately 500 to 600 watts.

26. A process as claimed in any of claims 12 to 25, further comprising providing said oxygen at a flow rate between approximately 0-400 sccm.

27. A process as claimed in any of claims 12 to 26, further comprising providing said oxygen at a flow rate between approximately 0-150 sccm.

28. A process as claimed in any of claims 12 to 27, further comprising providing said helium at a flow rate between approximately 0-5000 sccm, and said nitrogen at a flow rate between approximately 0-5000 sccm.

29. A proces for capping an extremely low dielectric constant ("ELK") film using a silicon carbide material comprising:

forming an ELK film on a substrate; and

depositing a silicon carbide capping layer having a dielectric constant of approximately less than 5 on said ELK film, where said silicon-carbide layer is produced by a process providing a silicon containing precursor, a carbon containing precursor and process gases comprising oxygen, helium and nitrogen at rates of 0-400 sccm, 0-5000 sccm, and 0-5000 sccm respectively for a process gases, and providing said silicon containing precursor and said carbon containing precursor at rate approximately six times that of the oxygen and further comprising reacting said silicon and said carbon in a chamber having pressure in the range of 1 to 15 Torr with an RF power source supplying a power at a rate of approximately 300-600 watts and a substrate surface temperature between 100° to approximately 450°C and having a shower head to substrate spacing of approximately 200 to approximately 600 mils, and where said capping layer has an adhesion strength of at least 35 Mpa and said ELK film, and where the dielectric constant of the for a stack consisting of said ELK film and said silicon carbide layer is at most approximately 3.0.

30. A substrate having a capped extremely low dielectric constant ("ELK") layer, comprising:

a semiconductor substrate;

an ELK layer deposited on said substrate; and

a silicon carbide type layer deposited on said ELK layer.

31. A substrate as claimed in claim 30, wherein said silicon carbide type layer has an effective dielectric constant of approximately less than 5.

32. A substrate as claimed in claim 29 or claim 31, wherein said silicon carbide type layer is a carbon doped oxide capping layer which has an effective dielectric constant of approximately less than 3.5.

33. A substrate as claimed in any of claims 29 to 32, wherein the dielectric constant of the stack consisting of said ELK film and said silicon carbide layer is approximately less than 3.

34. A substrate as claimed in any of claims 29 to 33, wherein the dielectric constant of the stack consisting of said ELK film and said silicon carbide layer is approximately less than 2.5.

35. A substrate as claimed in any of claims 29 to 34, wherein said silicon carbide layer comprises an etch selectivity ratio of between 40 to 1 to 1 to 1.

36. A substrate as claimed in any of claims 29 to 35, wherein said silicon carbide layer has an adhesion strength to said ELK layer of at least 35 Mpa.

37. A substrate as claimed in any of claims 29 to 36, wherein said silicon carbide layer is a moisture resistant layer.

38. A substrate as claimed in any of claims 29 to 34, wherein said silicon carbide layer is produced by a process providing a silicon containing precursor, a carbon containing precursor and process gases comprises oxygen, helium and nitrogen at rates of 0-400 sccm, 0-5000 sccm, and 0-5000 sccm respectively for the process gases, and providing said silicon containing precursor and said carbon containing precursor at rate approximately six times that of the oxygen and further comprising reacting said silicon and said carbon in a chamber having pressure in the range of 1 to 15 Torr with an RF power source supplying a power at a rate of approximately 300-600 watts and a substrate surface temperature between 100° to approximately 450°C and having a shower head to substrate spacing of approximately 200 to approximately 600 mils.

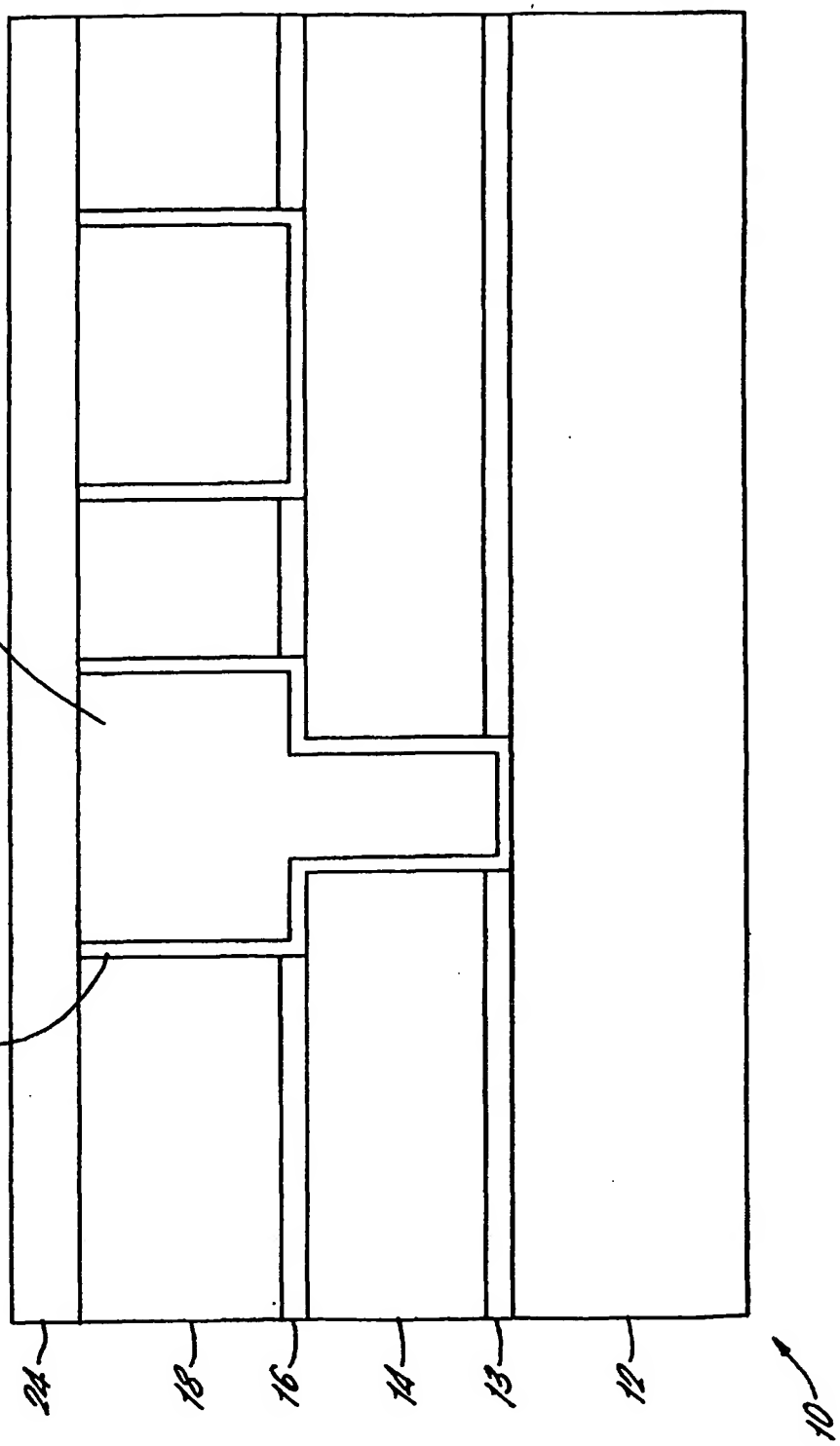


FIG. 1.

FIG. 2.

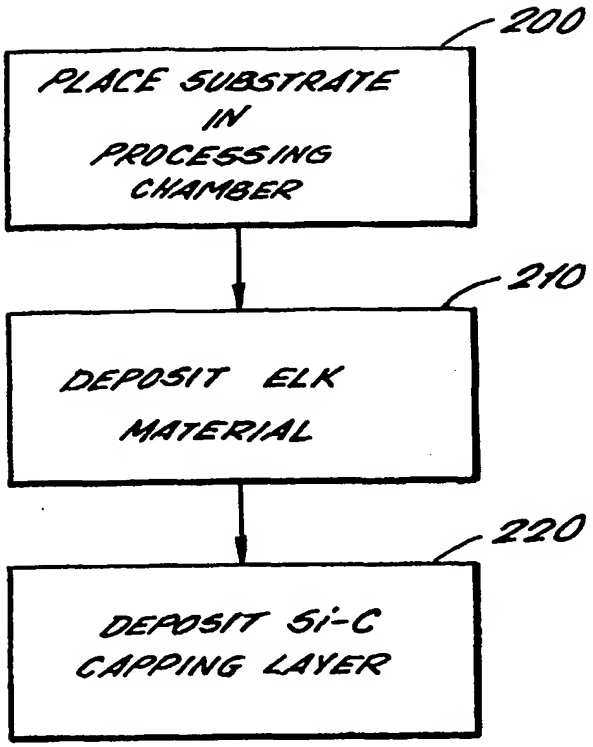
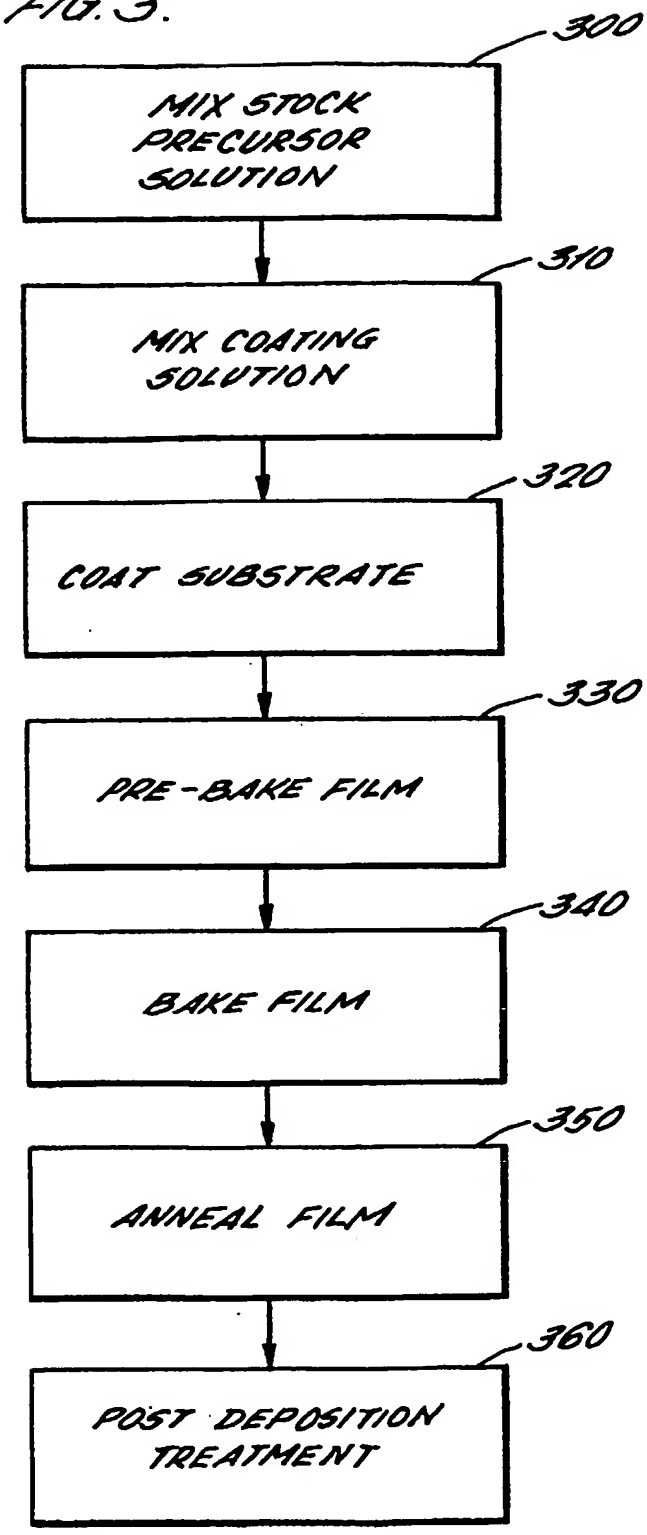

200
PLACE SUBSTRATE IN PROCESSING CHAMBER
210
DEPOSIT ELK MATERIAL
220
DEPOSIT Si-C CAPPING LAYER

FIG. 3.


300
MIX STOCK PRECURSOR SOLUTION
310
MIX COATING SOLUTION
320
COAT SUBSTRATE
330
PRE-BAKE FILM
340
BAKE FILM
350
ANNEAL FILM
360
POST DEPOSITION TREATMENT